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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,695	02/01/2002	Sribalan Santhanam	5580-04900	1574

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/061,695	SANTHANAM ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 10-20* is/are rejected.

7)☐ Claim(s) *4-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/02 & 4/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-20 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway, U.S. Patent No. 6,536,024, in view of Piazza, U.S. Patent No. 6,393,579.

As per claim 15, Hathaway teaches an apparatus comprising:

a first circuit including at least a first subcircuit and a second subcircuit (fig. 1a, domain 106 includes subdomains 104 and 106; col. 7, lines 48-57); and

a clock tree having a clock input, a control input , and a plurality of clock outputs (fig. 2f, portion of clock tree to medium domain has SCLK and control inputs to an AND gate, and a plurality of outputs; col. 8, lines 7-14), at least a first clock output of the plurality of clock outputs coupled to the first subcircuit and at least a second clock output of the plurality of clock outputs coupled to the second subcircuit (let medium domain of fig. 2f correspond to domain 106 of fig. 1a);

wherein the plurality of clock outputs are collectively conditionally gated from the clock input responsive to the control input (fig. 1a, signal CLKG_B controls gate 119).

However, Hathaway does not expressly teach at least some of the plurality of clock outputs are individually conditionally gated from the clock input further responsive

to circuitry monitoring activity in the respective subcircuits. Piazza teaches gating at least some of a plurality of clocks responsive to activity in respective subcircuits (fig. 1, respective pipeline stages of a circuit receive individual clocks; col. 3, line 59 – col. 4, line 1, stages gated responsive to activity; fig. 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Piazza's subcircuit clock gating to Hathaway's first circuit. A motivation for doing so would have been to reduce power consumption while the overall first circuit is active (Piazza, col. 2, lines 21-32).

As per claim 16, Hathaway teaches a second circuit coupled to the control input, the second circuit configured to generate the control input responsive to an event (fig. 1a, control unit 119 generates CLKG_B;.col. 2, lines 28-36). Because Piazza teaches a plurality of pipeline stages that require a plurality of clock cycles to process data, the clock tree must not be gated for a plurality of clock cycles. Piazza teaches the circuitry monitoring activity operates on a clock cycle by clock cycle basis (fig. 2; col. 5, lines 11-19).

As per claim 17, Hathaway teaches the clock tree comprises a plurality of levels of clock buffer circuitry, and wherein a first level of the plurality of levels includes one or more logic gates which combine the clock input and the control input (fig. 2f).

As per claim 18, Hathaway teaches any number of the plurality of levels (col. 8, lines 7-14).

As per claim 19, Hathaway teaches apparatus as recited in claim 15 further comprising:

a second circuit including at least a third subcircuit and a fourth subcircuit (fig. 1a, domain 107 may have subdomains such as those in domain 105); and

a second clock tree having a second clock input, a second control input, and a second plurality of clock outputs (fig. 2f, portion of clock tree to large domain has SCLK and control inputs to an AND gate, and a plurality of outputs), at least a third clock output of the second plurality of clock outputs coupled to the third subcircuit and at least a fourth clock output of the second plurality of clock outputs coupled to the fourth subcircuit (let large domain of fig. 2f correspond to domain 107 of fig. 1a).

Piazza teaches gating at least some of a plurality of clocks responsive to activity in respective subcircuits (fig. 1, respective pipeline stages of a circuit receive individual clocks; col. 3, line 59 – col. 4, line 1, stages gated responsive to activity; fig. 3).

As per claim 20, since Hathaway/Piazza teaches the apparatus of claim 15, Hathaway/Piazza teaches the claimed carrier medium.

3. Claims 1-3, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander et al., U.S. Patent No. 5,539,681 ("Alexander"), in view of Hathaway, U.S. Patent No. 6,536,024, and Piazza, U.S. Patent No. 6,393,579.

As per claim 1, Alexander teaches a processor comprising:

an execution circuit configured to execute an instruction (fig. 1, such as fixed point unit 22, load/store unit 24, or floating point unit 26);

an issue circuit coupled to the execution circuit (fig. 1, instruction dispatch unit 18), wherein the issue circuit is configured to issue an instruction to the execution circuit (col. 5, lines 38-41), and wherein the issue circuit is configured to generate a control

signal responsive to whether or not the instruction is issued to the execution circuit (fig. 2a; col. 7, lines 15-48, via hold lines 82a-c); and

a clock distribution network for clocking circuitry in the processor, wherein a portion of the clock distribution network supplies clock signals the execution circuit (col. 9, lines 10-14), the portion of the clock distribution network coupled to receive the control signal for conditionally gating the clock signals (fig. 3; col. 10, lines 30-38; col. 11, lines 7-13)

However, Alexander does not expressly teach the clock distribution network as a tree that supplies a plurality of clocks to an execution network. Hathaway teaches that clock distribution networks in processor are commonly configured as trees (col. 2, lines 11-27) that supply a plurality of clocks to domains, or logic circuitry (fig. 1a; col. 8, lines 7-14; fig. 2f). Hathaway teaches also a logic circuitry block including at least first and second subcircuits (fig. 1a, domain 106 includes subdomains 104 and 106; col. 7, lines 48-57; let medium domain of fig. 2f correspond to

domain 106 of fig. 1a). At the time of the invention, the time of the invention, it would have been obvious to one of ordinary skill in the art to implement Alexander's clock distribution network as a clock tree, as clock trees are well known in the art for distributing system clocks.

Alexander/Hathaway does not expressly teach conditionally gating at least some of the plurality of clocks responsive to activity in the respective subcircuits of the execution circuit. Piazza teaches gating at least some of a plurality of clocks responsive to activity in respective subcircuits (fig. 1, respective pipeline stages of circuit receive individual clocks; col. 3, line 59 – col. 4, line 1, stages gated responsive to activity; fig.

3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Piazza's subcircuit clock gating to Alexander/Hathaway's execution unit. A motivation for doing so would have been to reduce power consumption while the overall execution unit is active (Piazza, col. 2, lines 21-32).

As per claim 2, Alexander teaches the issue circuit is configured to generate the control signal for gating the execution unit according to when there are instructions for the particular execution unit (fig. 2a). Because Piazza teaches a plurality of pipeline stages that require a plurality of clock cycles to process data, the clock tree must not be gated for a plurality of clock cycles.

As per claim 3, Piazza teaches the clock tree is configured to individually gate the plurality of clocks on a clock cycle by clock cycle basis (fig. 2; col. 5, lines 11-19).

As per claim 10, Alexander teaches the execution circuit comprises a floating point unit (fig. 1, floating point unit 26).

As per claim 13, Alexander teaches the execution circuit comprises circuitry for executing a load/store instruction (fig. 1, load/store unit 24).

As per claim 14, Alexander teaches the execution unit comprises a data cache (fig. 1, data cache 32).

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander/Hathaway/Piazza, as applied to claim 10 above, further in view of Nakano, U.S. Patent No. 4,797,849.

As per claim 11, Alexander/Hathaway/Piazza is silent with respect to functions performed by the subcircuits of the floating point unit. Nakano teaches a floating point

pipeline comprising an adder circuit and a multiplier circuit (fig. 1, adder 14 and multiplier 11). At the time of the invention, it would have been obvious to one of ordinary skill in the art that the pipeline stages of Piazza may comprise an adder and a multiplier as such functions are well known in the art.

As per claim 12, Nakano teaches a third subcircuit that includes an approximation circuit (fig. 1, approximation circuit 10).

Allowable Subject Matter

5. Claims 4-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 21, 2004

THOMAS LEE
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